The 13th International Workshop on High-Performance, Power-Aware Computing (HPPAC'17)

https://sites.google.com/site/hppac17/home

Program co-chairs: Shuaiwen Leon Song, Pacific Northwest National Lab
Richard Vuduc, Georgia Tech
Publicity Chair: Shirley Moore, Oak Ridge National Laboratory

Proceedings Chair: Joseph Manzano, Pacific Northwest National Lab

Venue

To be held on Monday, May 29, in conjunction with IPDPS 2017.

Overview

Power and energy are now recognized as first-order constraints in high-performance computing. Optimizing performance under power and energy bounds requires coordination across not only the software stack (compilers, operating and runtime systems, job schedulers) but also coordination with cooling systems and outwards to electrical suppliers. As we continue to move towards exascale and extreme scale computing, understanding how power translates to performance becomes an increasingly critical problem.

The purpose of this workshop is to provide a forum where cutting-edge research in the above topic can be shared with others in the community. We welcome submissions addressing power aware computing issues. All papers will be subject to single-blind peer review, and the quality of standard papers is expected to be high.

Topics of particular interest include (but are not limited to):

* Performance optimization under node, job, cluster and site power bounds
* Power/performance tradeoffs across accelerators, processors and DRAM
* Cooling/performance tradeoffs
* Translating budgetary bounds into power and energy bounds.
* Power-efficient system design, from computer center to silicon
* Effects of compiler optimizations on application power and energy efficiency
* Power- and energy-aware job schedulers, runtime systems and operating systems
* Models of power and performance, from processors and components to computer centers
* Evaluations of hardware power and energy controls
* Applications specific power and energy optimization

Submission Guidelines

Papers should not exceed ten single-spaced pages (including figures, tables and references) using 12-point font on 8½x11-inch pages. Submissions will be judged on correctness,

originality, technical strength, significance, presentation quality, and relevance. Submitted papers should not have appeared in or be under consideration for another venue. A full peer-review process will be followed with each paper being reviewed by at least three members of the program committee.

Submissions should follow the IEEE Conference Proceedings templates found at http://www.ieee.org/conferences_events/conferences/publishing/templates.html Camera-ready copy will need to conform to IPDPS guidelines; these will be announced during author notification.

Important dates

Paper Submission: January 29th
Paper Notification: February 22nd
Final Paper Due: March 7th